components, elements, modules or units may use a direct circuit structure, such as a memory, a processor, a logic circuit, a look-up table, etc. that may execute the respective functions through controls of one or more microprocessors or other control apparatuses. Also, at least one of these components, elements, modules or units may be specifically embodied by a module, a program, or a part of code, which contains one or more executable instructions for performing specified logic functions, and executed by one or more microprocessors or other control apparatuses. Also, at least one of these components, elements, modules or units may further include or may be implemented by a processor such as a central processing unit (CPU) that performs the respective functions, a microprocessor, or the like. Two or more of these components, elements, modules or units may be combined into one single component, element, module or unit which performs all operations or functions of the combined two or more components, elements, modules or units. Also, at least part of functions of at least one of these components, elements, modules or units may be performed by another of these components, elements, modules or units. Further, although a bus is not illustrated in the above block diagrams, communication between the components, elements, modules or units may be performed through the bus. Functional aspects of the above exemplary embodiments may be implemented in algorithms that execute on one or more processors. Furthermore, the components, elements, modules or units represented by a block or processing steps may employ any number of related art techniques for electronics configuration, signal processing and/or control, data processing and the like.

[0478] Hereinabove, although the exemplary embodiments have been shown and described, it should be understood that the inventive concept is not limited to the disclosed embodiments and may be variously changed without departing from the spirit and the scope of the inventive concept. Therefore, the exemplary embodiments described above should be construed as including all the changes, equivalents, and substitutions included in the spirit and scope of the inventive concept.

What is claimed is:

1. A receiving apparatus receiving and processing a layered division multiplexing (LDM) signal, the receiving apparatus comprising:

a first decoder configured to decode a signal transmitted through a first layer from the LDM signal using a parity check matrix to generate low density parity check (LDPC) information word bits and parity bits;

an encoder configured to encode the LDPC information word bits, generated by decoding the signal transmitted through the first layer, using the parity check matrix to generate parity bits corresponding only to preset columns in the parity check matrix; and

a second decoder configured to decode a signal obtained by removing, from the LDM signal, a signal corresponding to the LDPC information word bits generated by decoding the signal transmitted through the first layer, the parity bits generated by the encoder, and the parity bits generated by the first decoder except the parity bits generated by the encoder, thereby to generate information word bits transmitted through a second layer.

2. The receiving apparatus as claimed in claim **1**, wherein the preset columns are columns having a degree of 1 in the parity check matrix.

3. The receiving apparatus as claimed in claim **2**, wherein the parity check matrix comprises a first parity check matrix comprising a first information word partial matrix and a first parity partial matrix, which is a dual diagonal matrix, and a second parity check matrix comprising a second information word partial matrix and a second parity partial matrix which is a unit matrix, and

wherein the encoder generates the parity bits corresponding only to the columns having the degree of 1 in the parity check matrix.

4. The receiving apparatus as claimed in claim **1**, wherein the first decoder decodes the signal transmitted through the first layer from the LDM signal using a first LDPC decoder, and decodes the LDPC information word bits, corresponding to the signal transmitted through the first layer, using a first Bose, Chaudhuri, Hocquenghem (BCH) decoder to generate information word bits transmitted through the first layer.

5. The receiving apparatus as claimed in claim **4**, wherein the encoder encodes the LDPC information word bits, corresponding to the signal transmitted through the first layer, using an LDPC encoder to generate the parity bits corresponding only to the preset columns in the parity check matrix.

6. The receiving apparatus as claimed in claim **5**, wherein the encoder encodes the information word bits, transmitted through the first layer, using a BCH encoder to generate BCH parity bits, and

wherein the LDPC encoder encodes the information word bits transmitted through the first layer and the BCH parity bits to generate the parity bits corresponding only to the preset columns in the parity check matrix.

7. The receiving apparatus as claimed in claim **4**, wherein the second decoder decodes the signal obtained by the removing to generate LDPC information word bits and parity bits, corresponding to a signal transmitted through the second layer, using the first LDPC decoder, and decodes the LDPC information word bits, corresponding to the signal transmitted through the second layer, using the first BCH decoder to generate the information word bits transmitted through the second layer.

8. The receiving apparatus as claimed in claim **4**, wherein the second decoder decodes the signal obtained by the removing to generate LDPC information word bits and parity bits, corresponding to a signal transmitted through the second layer, using a second LDPC decoder, and decodes the LDPC information word bits, corresponding to the signal transmitted through the second layer, using a second BCH decoder to generate the information word bits transmitted through the second layer.

9. A decoding method of a receiving apparatus receiving and processing a layered division multiplexing (LDM) signal, the decoding method comprising:

decoding a signal transmitted through a first layer from the LDM signal using a parity check matrix to generate low density parity check (LDPC) information word bits and parity bits;

encoding the LDPC information word bits, generated by decoding the signal transmitted through the first layer,